Claims

[c1]   What is claimed is:

1. A serializer/deserializer (SERDES) circuit having built-in self-test (BIST) capabilities that is configured to perform jitter sensitivity characterization, comprising:

a CDR circuit coupled to said SERDES circuit that generates recovered clock and data from an incoming serial data stream;

a deserializer circuit connected to said CDR circuit to generate corresponding data (Parallel Data Out) and clock (DES clock) in a parallel format;

a programmable pattern generator generating BIST patterns;

a serializer circuit that receives either the BIST patterns or the input data (Parallel Data In) in a parallel format on its data input and an external clock (SER clock) on its clock input to generate a serial data stream;

a delay perturbation circuit for adding a perturbation delay to said serial data stream to produce a perturbed serial data stream;

a multiplexor circuit to output either the serial data stream or the perturbed serial data stream in a loop back to the CDR circuit;

a control logic circuit block coupled to said deserializer circuit to detect a start-of-frame pattern using a dedicated signal (FD) and coupled to the programmable pattern generator and the perturbation circuit.

[c2]   2. The serializer/deserializer (SERDES) circuit according to claim 1 further comprising a calibration circuit coupled to the output of said delay perturbation circuit.

[c3]   3. The serializer/deserializer (SERDES) circuit according to claim 1, wherein said delay perturbation circuit comprises a variable delay line and said perturbation comprises a variable delay.

[c4]   4. The serializer/deserializer (SERDES) circuit according to claim 3, wherein said variable delay comprises a sudden increase or decrease of the delay value of said variable delay line.

[c5]   5. The serializer/deserializer (SERDES) circuit according to claim 4, wherein said variable delay line comprises a plurality of DLL circuits, connected in series and coupled to said serial data stream.

[c6]   6. The serializer/deserializer (SERDES) circuit according to claim 5, wherein the signal obtained at the output of said series of a plurality of DLL circuits is used as a calibration signal to be applied to a calibration circuit.

[c7]   7. The serializer/deserializer (SERDES) circuit according to claim 6 further comprising a calibration circuit comprising a latch having its clock input connected to said calibration signal and a data input driven by the serializer clock.

[c8]   8. The serializer/deserializer (SERDES) circuit according to claim 7 wherein said calibration signal corresponds to a delay equal to the serializer clock half-period.

[c9]   9. A method of characterizing the jitter sensitivity of a clock and data recovery (CDR) circuit connected in series with a deserializer circuit within a serializer/deserializer (SERDES) circuit having built-in self-test (BIST) capabilities comprising the steps of:

generating a serial data stream by the serializer that is continuously applied to the CDR circuit and the deserializer;

inserting a first start-of-frame pattern in the serial data stream;

adding a perturbation delay to said serial data stream to produce a perturbed serial data stream;

inserting a second start-of-frame pattern in the serial data stream; and

determining whether the deserializer has detected whether said second start-of-frame pattern has the

same bit alignment as the first start-of-frame pattern.

[c10] 10. The method according to claim 9, wherein said serial data stream is a BIST pattern generated by a programmable pattern generator.

[c11] 11. The method according to claim 10 wherein said perturbation is applied continuously to generate a plurality of delay increments to simulate jitter characteristics of said serial data stream.